1. GENERAL DESCRIPTION

iCatch's CR3A SoC integrates advanced image signal processor (ISP), 300MP/s video encoder/decoder (Video CODEC), neural processing unit (NPU), video and audio digital signal processor (VDSP/ADSP), USB3.2 Gen1 connectivity, and Security Engine in a low power single chip design. The ISP and Video CODEC function as the foundation of the automotive imaging system, along with the integrated multi-camera sensor interface making CR3A an expandable solution for multi-channel automotive imaging application, such as dash camera, driver and in-cabin monitoring and electronic mirror systems. To add extra features to improve user experience and safety, the embedded NPU and VDSP can be used to implement ADAS functions, such as driver monitoring system (DMS), blind spot detection (BSD) and rear collision warning (RCW).

The CR3A SoC also includes a series of security features in the Security Engine, such as secure boot, hardware programmable security level for peripheral interfaces, data encryption and protection with a complete set of cypher coding engines, true random number generator (TRNG), and one-time programmable (OTP) memory. User data can be securely protected by incorporating these security functions into system design.

iCatch has developed software development kits (SDK) specifically for automotive imaging on CR3A SoC. Moreover, a full set of optimized neural network tool chains are also available for customers to port 3rd parties' or in-house developed neural network models onto CR3A SoC to efficiently add AI features to the cameras to accelerate the time-to-market cycle.

2. FEATURES

2.1. Image Sensor Interface

- Up to four sensor inputs via virtual channels
- Support MIPI D-PHY/sLVDS/HiSPi up to 1.5Gbps per lane

2.2. Advanced Image Processing

- Pixel processing speed up to 240M pixels/sec
- Real-time multi-frame fusion video HDR
- Local tone mapping (LTM) for direct HDR sensor
- AI-enhanced denoise engine supporting 4K video
- RCCB and 4X4 RGB-IR de-mosaic with HDR and LTM support
- Event-based Vision Sensor (EVS) support

2.3. Video CODEC

- H.264 BP/MP/HP and H.265 MP up to level 5
- Real-time encode/decode up to 300M pixels/s
- Up to 8 simultaneous encoding streams
- Advanced bitrate control in CBR and VBR mode

2.4. Processor Cores

- Dual-core ARM Cortex-A7 processors up to 720MHz
- NPU with computation power up to 1.2TOPS
- Video DSP (MAE) for NPU pre/post processing
- AON controller for ultra-low power applications

2.5. Audio

- Digital PDM microphone input.
- Internal CODEC with mono input and mono line output
- Built-in audio DSP for AEC, ALC, ANR
- I2S interface to external audio codec

2.6. Memory/Storage

- Programmable DRAM speed up to 1 GHz
- Support SPI NAND and NOR flash with 1/2/4/8-bit data bus
- Support SD/SDHC/SDXC and eMMC interfaces

2.7. Security

- Support secure boot
- Support AES/DES/3DES encryption standards
- True random number generators
- Include 4K-bit OTP memory

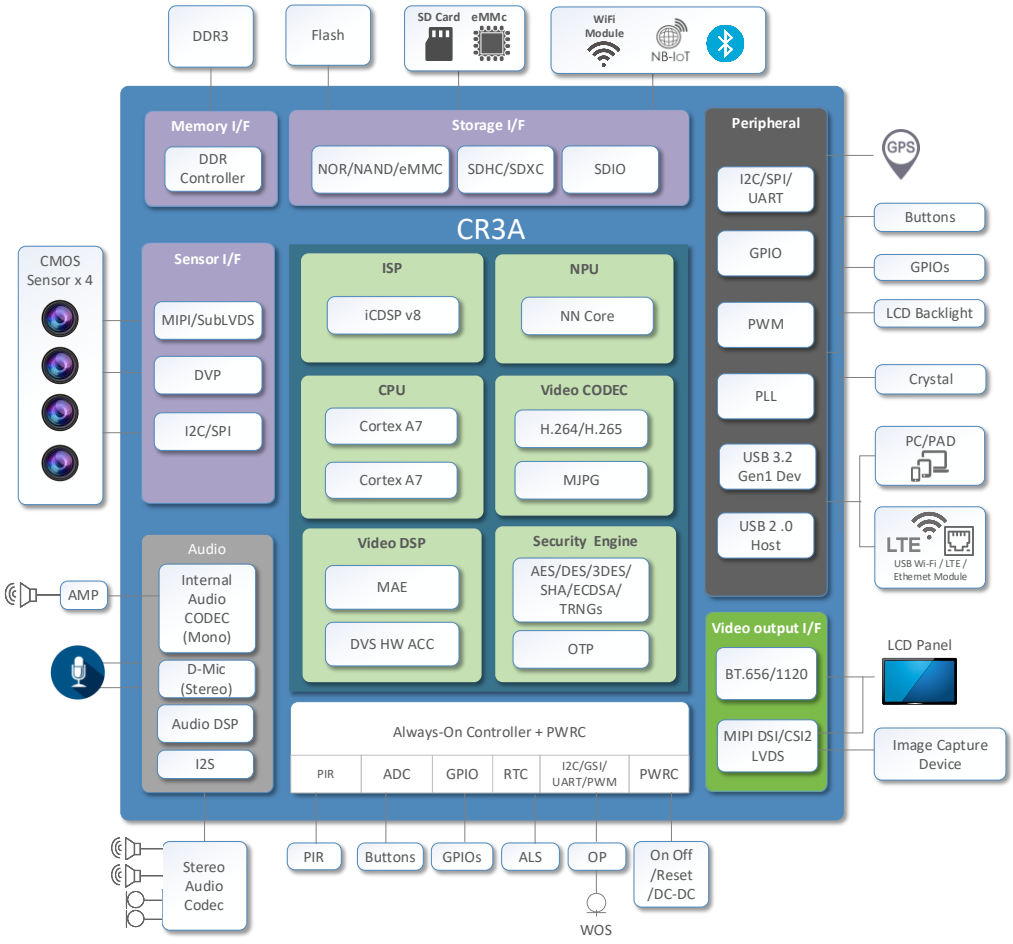
2.8. Peripherals

- USB 3.2 G1 device and USB 2.0 host interfaces
- GPIO, PWM, UART, SPI, and I2C ports
- Real-time clock and watch-dog timer
- Multiple channels of 10-bits SAR ADC
- SDIO controller for WiFi module

2.9. Package

- LFBGA-305, 13 x 13 x 1.5 mm
- AEC-Q100 Grade 2 (-40°C~105°C)

3. BLOCK DIAGRAM



4. DEVELOPMENT PLATFORM

- Evaluation board (EVB)
- Software development kits (SDK)
- Documentations

4.1. Evaluation Board

- CR3A main evaluation board (EVB)
- Sensor board, LCD panel board, audio board

4.2. Software Development Kits

- ISP, 3A, NDK Libraries
- WiFi video application reference design source code
- PC tool chains (Programmer, font and string generators)
- Android/iOS mobile phone APP SDK

4.3. Documentations

- EVB user manual, application notes and API documents
- Datasheet, schematics and layout files