

PICA[®] 200 3D Graphics IP



High detail, high speed, low power consumption real-time 3D graphics



PICA200 graphics IP core is a 3D graphics IP core for embedded applications with DMP's proprietary extension MAESTRO that realizes a flexible, scalable, and innovative high quality graphics to meet broad demand for ASIC/ASSP/SoC (System on Chip) applications for the rapidly growing "21st-century Digital Consumer Market" such as amusement machines, car infotainment systems, mobile phones, game consoles, and digital appliances.

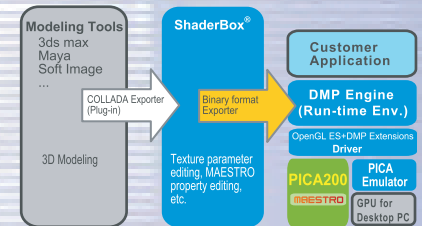
PC-grade sophistication and high-speed rendering in embedded devices

DMP offers the "DMP MAESTRO technology", an advanced rendering extension that implements various modeled CG algorithms as hardware. DMP MAESTRO technology not only allows for beautiful graphics and reduced content size and memory bandwidth, but also for reduced power consumption at the system level.



Tools for efficient content creation

DMP provides PICA emulators for PC environments, "ShaderBox[®]" which is an authoring support tool for DMP extensions, and content execution environments (engines). All these tools support the industry standard COLLADA specification, allowing for seamless workflow from major CG tools as well as efficient and low-cost production of contents that make full use of DMP extensions.



Graphics chip development support service

DMP, with its superior chip development expertise proven in the development of "ULTRAY2000" or the "NV7" 3D/2D graphics LSI for NIFCO Advanced Technology Inc., offers support service for the development of ASSPs /ASCPs with DMP's graphics IP.



Main features / Specifications

PICA200 adds OpenGL ES 1.1 functions and DMP extensions, including the following:

- Frame buffer: Maximum 4095x4095 pixels
- Pixel format: RGBA4444, RGB565, RGBA5551, RGBA8888
- Vertex program (ARB_vertex_program)
- Render to texture
- mipmap
- Bilinear texture filtering
- Alpha blending
- Full-scene antialiasing (2x2)
- Polygon offset
- 8-bit stencil buffer
- 24-bit depth buffer
- Single/Double/Triple buffer
- Vertex performance: Maximum 15.3M polygons/sec (at 200MHz)
- Pixel performance: Maximum 800M pixels/sec (at 200MHz)

<DMP MAESTRO technology>

- Per-pixel lighting
- Procedural texture
- Refraction mapping
- Subdivision primitive
- Shadow
- Gaseous object rendering