

PICA[®]200 Lite 3D Graphics IP



Digital appliances, car electronics, mobile devices, etc.



Industrial equipment for low-volume manufacturing and/or long-term supply

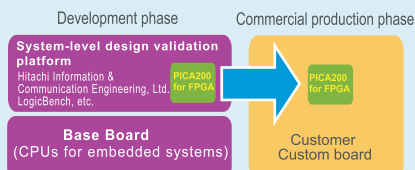
3D user interface creation tools and partnership

DMP is strengthening its collaboration with 3D-UI creation tool vendors to support planning and development of products using PICA200 Lite at the system level from both the hardware and software perspectives.



FPGA system development partnership

DMP is strengthening its cooperation with system-level design validation platform vendors for FPGA-based systems to support efficient development of systems using PICA200 for FPGA.



PICA200 Lite is a 3D graphics IP core with functions optimized for UI applications that inherits the already proven characteristics of PICA200 such as super low power consumption and high performance, but with further reduction in power consumption and dimensions.

3D-UI solution for embedded devices supporting full HD resolution and industry standard OpenGL ES

PICA200 Lite supports the industry's largest (survey by DMP) full HD resolution (1920x1080 pixels) to meet the need for wider displays and larger screens in the market of digital appliances, car electronics, mobile devices, and industrial equipment etc., and realizes a high performance and high quality 3D graphics UI.

PICA200 Lite is compliant with OpenGL ES 1.1, the industry standard API created by Khronos Group, which enables the reuse of existing software assets.



Industry's first IP solution for FPGA with full 3D graphics

PICA200 Lite also supports applications using FPGA for the purpose of securing low-volume manufacturing and/or long-term supply of industrial, medical, and aerospace-related equipments etc. With DMP's IP solution for FPGA, it is now possible to realize sophisticated HMIs (Human Machine Interfaces) with real-time 3D graphics on these type of equipment.

Main features / Specifications

- API support: OpenGL ES 1.1
- Frame buffer: Maximum 4095x4095 pixels
- Pixel format: RGBA4444, RGB565, RGBA5551, RGBA8888
- Vertex program (ARB_vertex_program)
- Render to texture
- mipmap
- Bilinear texture filtering
- Alpha blending
- Full-scene antialiasing (2x2)
- Line antialiasing
- Polygon offset
- 8-bit stencil buffer
- 24-bit depth buffer
- Single/Double/Triple buffer
- Supported FPGA: Xilinx® Virtex®-5 (Support for Altera Stratix® III and others planned)
- Vertex performance: Maximum 12.7M polygons/sec (at 166MHz)
Maximum 3.8M polygons/sec (for FPGA 50MHz)
- Pixel performance: Maximum 166M pixels/sec (at 166MHz)
Maximum 50M pixels/sec (for FPGA 50MHz)



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